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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/665,422 | 09/20/2000 | Bin Zhao | | 7422 |

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| EXAMINER | |
|---|---|
| DIAZ, JOSE R | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2815 | |

DATE MAILED: 04/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/665,422 | ZHAO ET AL. | |
| | Examiner | Art Unit | |
| | José R. Díaz | 2815 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *16 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-8 and 21-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 21-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-8 and 29-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Buchwalter et al. (US Pat. No. 6,184,121 B1).

Regarding claims 1-2 and 29, Buchwalter et al. teaches a method for fabricating a damascene interconnect structure having one or more air trenches and a plurality of spaced-apart metal lines comprising:

(a) fabricating the damascene structure to a via level through a processing step prior to forming contact vias (90) (see fig. 4A), wherein step (a) comprises:

depositing a first dielectric layer (20) (see fig. 2C);

depositing a first capping layer (30) over the first dielectric layer (see fig. 2C);

forming a plurality of trenches (40, 50) in the first capping layer (30) and the first dielectric layer (20) (see fig. 2A and col. 2, lines 3-4)[1];

[1] In column 2, lines 3-4, Buchwalter et al. expressly teaches the formation of "vias" in the dielectric layer (20). Please note that the term "vias" is the plural form of the term via which means more than one via. Thus, Buchwalter et al. anticipates the recited limitation of forming a plurality of trenches in the first

filling the plurality of trenches with metal to form the plurality of spaced-apart metal lines (70), wherein the plurality of spaced-apart metal lines are situated in the first capping layer and the first dielectric layer (Please note that trenches 50 and vias 40 are filled with metal (70). See fig. 2A and col. 2, lines 9-10 and 13-15);

depositing a second capping layer (20) over the first capping layer (30) (see fig. 2D), wherein the second capping layer is situated over the selected metal lines (70) shown in fig. 2C);

depositing a second dielectric layer (30) over the second capping layer (20) (see fig. 2D); and

depositing a third capping layer (20) over the second dielectric layer (30) (Not shown)[2];

(b) etching one or more air trenches into the damascene structure so that the air trenches are positioned between selected metal lines (70) (see fig. 4A and col. 6, lines 53-61. Also consider the air trenches (110) shown in figure 4C, attached below);

(c) depositing a sealing layer (120) over the damascene structure having air trenches to seal the air trenches (110) (see fig. 4C); and

(d) depositing a polish or etch stop layer (130) over the sealing layer (see fig. 4C).

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capping layer (consider trenches (50) in figure 2A) and vias in the dielectric layer (consider vias 40 in column 2, line 4 and figure 4C, attached hereto).

[2] Please note that the sequence of steps for forming the structure shown in figure 2C can be repeated several times until the necessary number of wiring layers are built (col. 2, lines 20-22). For example, the steps can be repeated three times so that a multilevel structure comprising three pairs of insulating layers 20 and 30 is formed.

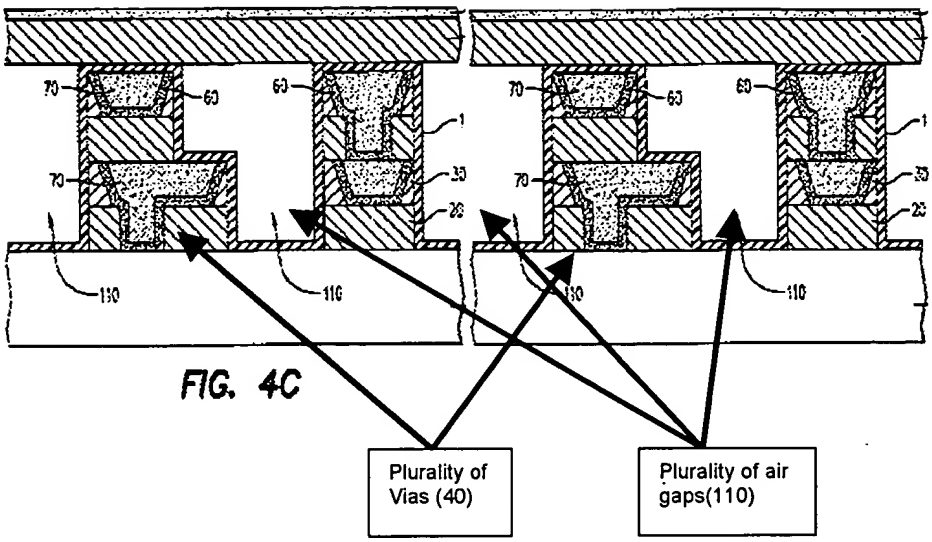


FIG. 4C

Regarding claims 3 and 30, Buchwalter et al. further teaches etching an air trench in the first and second dielectric layers, and the first, second and third capping layers (see fig. 4A and also, consider air trench (110) in figure 4C, attached above).

Regarding claims 4-8, Buchwalter et al. further teaches:

forming a via in the sealing layer (120) and the damascene structure (100) (consider the opening formed in layers 100, 120 and 130 as shown in figure 4D);

forming a trench over the sealing layer (consider the opening formed in the layer 130 as shown in figure 4D); and

forming a conductive layer (90), which forms a conductive layer (upper portion of the conductive layer) in the opening formed in layer (130) and a metal plug (bottom portion of the conductive layer) in the opening formed in layers (100) and (120) (see fig. 4D).

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 21-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Buchwalter et al. (US Pat. No. 6,184,121 B1) in view of Jeng (US Pat. No. 5,708,303).

Regarding claims 21-22, Buchwalter et al., as stated before, teaches a method for fabricating a damascene interconnect structure having one or more air trenches and a plurality of spaced-apart metal lines comprising:

(a) fabricating the damascene structure to a via level through a processing step prior to forming contact vias (90) (see fig. 4A), wherein step (a) comprises:

depositing a first dielectric layer (20) (see fig. 2C);

depositing a first capping layer (30) over the first dielectric layer (see fig. 2C);

forming a plurality of trenches (40, 50) in the first capping layer (30) and the first dielectric layer (20) (see fig. 2A and col. 2, lines 3-4)[3];

filling the plurality of trenches with metal to form the plurality of spaced-apart metal lines (70), wherein the plurality of spaced-apart metal lines are

[3] In column 2, lines 3-4, Buchwalter et al. expressly teaches the formation of "vias", the plural form of the term via which means more than one via, in the dielectric layer (20). Thus, Buchwalter et al. anticipates the recited limitation of forming a plurality of trenches in the first capping layer (consider trenches (50) in figure 2A) and vias in the dielectric layer (consider vias 40 in column 2, line 4 and figure 4C, attached hereto).

situated in the first capping layer and the first dielectric layer (Please note that trenches 50 and vias 40 are filled with metal (70). See fig. 2A and col. 2, lines 9-10 and 13-15);

depositing a second capping layer (20) over the first capping layer (30) (see fig. 2D), wherein the second capping layer is situated over the selected metal lines (70) shown in fig. 2C);

depositing a second dielectric layer (30) over the second capping layer (20) (see fig. 2D); and

depositing a third capping layer (20) over the second dielectric layer (30) (Not shown)[4];

(b) etching one or more air trenches into the damascene structure so that the air trenches are positioned between selected metal lines (70) (see fig. 4A and col. 6, lines 53-61);

(c) depositing a sealing layer (120) over the damascene structure having air trenches to seal the air trenches (110) (see fig. 4C); and

(d) depositing a polish stop layer (130) over the sealing layer (see fig. 4C).

However, Buchwalter et al. is silent with respect to depositing an etch stop layer directly on the polish stop layer. Jeng teaches that it is well known in the art to deposit an etch stop layer (50) directly on the polish stop layer (52) (see fig. 4).

[4] Please note that the sequence of steps for forming the structure shown in figure 2C can be repeated several times until the necessary number of wiring layers are built (col. 2, lines 20-22). For example, the steps can be repeated three times so that a multilevel structure comprising three pairs of insulating layers 20 and 30 is formed.

Buchwalter et al. and Jeng are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to deposit an etch stop layer directly on the polish stop layer. The motivation for doing so, as is taught by Jeng, is controlling trench depth (col. 3, lines 34-38). Therefore, it would have been obvious to combine Jeng with Buchwalter et al. to obtain the invention of claims 21-28.

Regarding claim 23, Buchwalter et al. further teaches etching an air trench in the first and second dielectric layers, and the first, second and third capping layers (see fig. 4A).

Regarding claims 24-28, Buchwalter et al. further teaches:

forming a via in the sealing layer (120) and the damascene structure (100) (consider the opening formed in layers 100 and 120 as shown in figure 4D);

forming a trench over the sealing layer (consider the opening formed in the layer 130 as shown in figure 4D); and

forming a conductive layer (90), which forms a conductive layer (upper portion of the conductive layer) in the opening formed in layer (130) and a metal plug (bottom portion of the conductive layer) in the opening formed in layers (100) and (120) (see fig. 4D).

### *Response to Arguments*

4. Applicant's arguments filed February 16, 2005 have been fully considered but they are not persuasive. In the instance case, Buchwalter et al., as stated before, anticipates and makes obvious the claimed invention by teaching the formation of a

plurality of vias in the dielectric layer (see column 2, lines 3-4), which is the new limitation incorporated in the claims and argued by applicant.

### *Conclusion*

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

### *Correspondence*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R. Díaz whose telephone number is (571) 272-1727. The examiner can normally be reached on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JRD
4/22/05

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER